Sierra Components, Inc.

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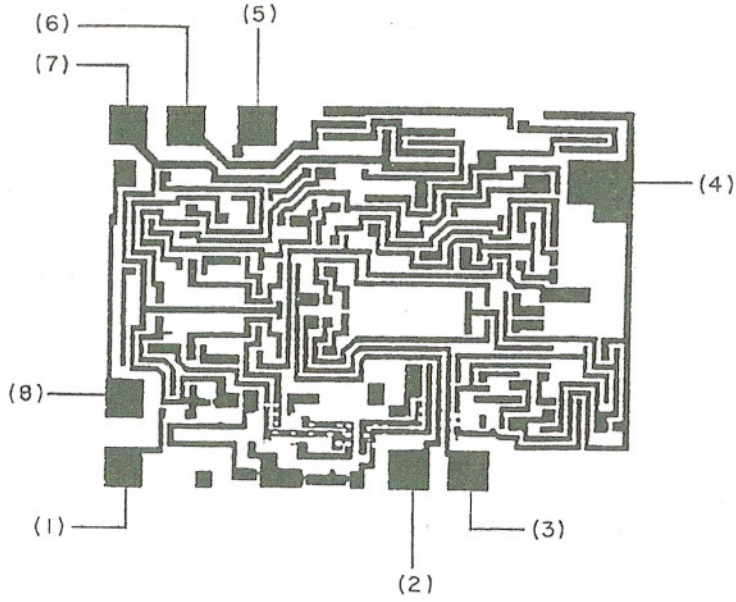
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PIN OUT TABLE					
PAD NO.	PACKAGE PIN NO.	DESCRIPTION	PAD NO.	PACKAGE PIN NO.	DESCRIPTION
1	1	BALANCE	5	11	BALANCE
2	3	-IN	6	12	OUT
3	4	+IN	7	13	+V
4	7	-V	8	15	COMP

METALLIZATION:
TOP _____ Al
BOTTOM _____ Si
DIE SIZE _____ 50 x 65 MIL
DIE THICKNESS _____ 19 ±1 MIL

Top Material: Al
Backside Material: Si
Bond Pad Size:
Backside Potential:
Mask Ref:

APPROVED BY: DG	**DIE SIZE : .050"x .065"**	**DATE: 2/7/07**
MFG: HARRIS	**THICKNESS:**	**P/N:HA-2520**